Translator's Statement

I Wei-Te Chung, a registered patent agent before the US Patent and Trademark Office (registration number: 43,325) who haves proficient knowledge of both English and Chinese, state that the translation of the priority document of CN Patent Application Case No. 03114064.5 is accurate to its original language.

Translator: _____
(Wei-Te Chung)

Date: Jan 4, 2006

Translation of CN Patent Application Case No. 03114064.5

Title

Method For Making A Field Emission Display

Abstract of the Invention

The present invention provides a method for making a field emission display. The method comprises the following steps: (1) providing a substrate; (2) depositing gate electrodes on the substrate corresponding to predetermined display pixels; (3) forming an insulating intermediate film on the gate electrodes; (4) depositing a catalyst layer on the insulating intermediate film; (5) forming an insulation layer on the catalyst layer, thereby defining spaces corresponding to the predetermined display pixels; (6) growing carbon nanotube arrays by chemical vapor deposition on the catalyst layer within the spaces defined by the insulation layer; (7) depositing cathode electrodes on the carbon nanotube arrays; (8) encapsulating the cathode plate and removing the substrate; (9) removing the insulation layer by a wet etching process; (10) packaging the cathode plate with a display screen including the anode electrodes.

Claims:

1. A method for fabricating a field emission display comprises the following steps:
   (1) providing a substrate;
   (2) depositing gate electrodes on the substrate corresponding to predetermined display pixels;
   (3) forming an insulating intermediate film on the gate electrodes;
   (4) depositing a catalyst layer on the insulating intermediate film;
   (5) forming an insulation layer on the catalyst layer, thereby defining spaces corresponding to the predetermined display pixels;
   (6) growing carbon nanotube arrays by chemical vapor deposition on the catalyst layer within the spaces defined by the insulation layer;
   (7) depositing cathode electrodes on the carbon nanotube arrays;
   (8) encapsulating the cathode plate and removing the substrate;
   (9) removing the insulation layer corresponding to the display pixels by a wet etching process;
   (10)packaging the cathode plate with a display screen including the anode electrodes.
2. The method for fabricating a field emission display of claim 1, characterized in that a protective layer of the gate electrodes is deposited on said substrate between steps (1) and (2).
3. The method for fabricating a field emission display of claim 2, characterized in that the thickness of the protective layer of the gate electrodes is in the range of 1μm~100μm.
4. The method for fabricating a field emission display of claim 2, characterized in that the manufacturing material of said protective layer of the gate electrodes is selected from the group consisting of: glass, metal coated with an insulation layer, silicon, silicon oxide, ceramic material and mica.
5. The method for fabricating a field emission display of claim 1, characterized in that a silicon protective layer is deposited on said insulating intermediate film between steps (3) and (4), and that said catalyst layer of step (4) is deposited on the silicon protective layer.
6. The method for fabricating a field emission display of claim 1, characterized in that the thickness of the insulating intermediate film is in

the range of 1μm~1000μm.

7. The method for fabricating a field emission display of claim 6, characterized in that the thickness of said insulating intermediate film is in the range of 10μm~200μm.
8. The method for fabricating a field emission display of claim 1, characterized in that the manufacturing material of said insulating intermediate film is selected from the group consisting of: glass, metal coated with an insulation layer, silicon, silicon oxide, ceramic material and mica.
9. The method for fabricating a field emission display of claim 5, characterized in that the thickness of said silicon protective layer is in the range of 10nm~1000nm.
10. The method for fabricating a field emission display of claim 5, characterized in that portions of said protective layer corresponding to the display pixels are removed by dry etching between steps (9) and (10).
11. The method for fabricating a field emission display of claim 1, characterized in that the manufacturing material of said insulation layer is selected from the group consisting of: glass, metal coated with an insulation layer, silicon, silicon oxide, ceramic material and mica.
12. The method for fabricating a field emission display of claim 1, characterized in that the thickness of said insulation layer is in the range of 1μm~10mm.
13. The method for fabricating a field emission display of claim 12, characterized in that the thickness of said insulation layer is in the range of 10μm~500μm.
14. The method for fabricating a field emission display of claim 1, characterized in that a layer of negative feedback resistance is deposited on the carbon nanotube arrays first and then cathode electrodes are deposited on the layer of negative feedback resistance in step (7).
15. The method for fabricating a field emission display of claim 14, characterized in that the manufacturing material of the layer of negative feedback resistance is selected from the group consisting of silicon and alloy.
16. The method for fabricating a field emission display of claim 1, characterized in that the thickness of said catalyst layer is in the range of 1nm~10nm.

17. The method for fabricating a field emission display of claim 16, characterized in that the thickness of said catalyst layer is 5nm.
18. The method for fabricating a field emission display of claim 1, characterized in that the catalyst layer corresponding to the display pixels is further removed by laser between steps (9) and (10).

Description of the Invention

【Field of the Invention】

The present invention relates to a field emission display device, and more particularly to a method for making a carbon nanotube based field emission display.

【Background of the Invention】

Carbon nanotubes are hollow carbon tubes, which were first discovered by Sumio Iijima in arc discharge products in 1991 and reported in Nature Vol. 354, p.56 published in 1991. For their characteristics such as great conductivity, perfect lattice structure, and micro-tips on the nanometer scale, carbon nanotubes have become a material with extremely good potential for field emission cathodes. Carbon nanotubes have broad prospects in many applications such as field emission display devices, electrical vacuum devices, and high power microwave devices.

Carbon nanotube arrays can be easily grown by chemical vapor deposition with a specified location, a specified direction and a specified height on a substrate such as a silicon substrate or a glass substrate. The size of the display pixels can achieve an extremely high accuracy by controlling the catalyst film in a semiconductor photolithography process. Thus, carbon nanotube arrays may be used rapidly in a flat panel display device.

US Pat. No. 6,339,281 discloses a method for making a triode-structure carbon nanotube based field emission display. The method comprises the following steps:

(1) forming cathodes on a substrate and then forming an insulation layer on the cathodes;

(2) forming a gate electrode layer, and then forming openings on the gate electrode layer;

(3) forming micro-cavities on the insulation layer **by photolithography** using the gate electrode layer as a mask;

(4) forming a catalyst layer on the substrate and growing carbon nanotube arrays on the catalyst layer by chemical vapor deposition.

However, in practical manufacturing processes, there are several disadvantages and insurmountable problems always present in making carbon nanotube arrays for field emission by chemical vapor deposition, as per the below:

1. In order to achieve a uniform illuminance, the distance between gate electrodes and carbon nanotube arrays used for field emission should be kept uniform on the millimeter scale over a large area. However, it is quite difficult to accomplish uniformity in heights of the carbon nanotubes over a large area by chemical vapor deposition.

2. For a portable flat panel display, energy consumption must be reduced. Further, in order to address and control the gray scale in the circuit easily, the threshold voltage of the gate electrodes should be as low as possible. Thus, the distance between the gate electrodes and the carbon nanotube arrays should be as short as possible. The heights the carbon nanotube arrays are grown to by chemical vapor deposition can be roughly controlled. However, the accuracy still cannot fulfill present-day requirements, and it is difficult to control the distance to be in a desirable range precisely.

3. The top surface of the carbon nanotube array grown by chemical vapor deposition inevitably contains a thin layer of randomly distributed carbon nanotubes with uneven diameters, and impurities such as a few catalyst particles and tiny amounts of amorphous carbon. These lead to instability and unevenness of the field emission performance, and may shorten the life of the device.

【Content of the Invention】

A technical problem to be solved by the present invention is to provide a method for fabricating a field emission display, wherein the distance between gate electrodes and carbon nanotube arrays is kept uniform on the millimeter scale over a large area.

A further technical problem to be solved by the present invention is to provide a method for fabricating a field emission display, wherein the

emitter ends of carbon nanotube arrays are uniform in diameter, arranged neatly, and free of impurities such as catalyst particles and amorphous carbon.

A still further technical problem to be solved by the present invention is to provide a method for fabricating a field emission display, wherein the distance between gate electrodes and carbon nanotubes is as short as possible; for instance, on the nanometer scale.

In order to solve the above-mentioned problems, the present invention provides a method for fabricating a field emission display. The method mainly comprises the following steps:

(1) providing a substrate;

(2) depositing gate electrodes on the substrate corresponding to predetermined display pixels;

(3) forming an insulating intermediate film on the gate electrodes;

(4) depositing a catalyst layer on the insulating intermediate film;

(5) forming an insulation layer on the catalyst layer, thereby defining spaces corresponding to the predetermined display pixels;

(6) growing carbon nanotube arrays by chemical vapor deposition on the catalyst layer within the spaces defining by the insulation layer;

(7) depositing cathode electrodes on the carbon nanotube arrays;

(8) encapsulating the cathode plate and removing the substrate;

(9) removing the insulation layer by a wet etching process;

(10) packaging the cathode plate with a display screen including the anode electrodes.

Between steps (1) and (2), a protective layer of the gate electrodes can be further deposited on the substrate so as to avoid carbon deposition on the gate electrodes in the growing process. Between steps (3) and (4), a silicon protective layer can be further deposited on the insulating intermediate layer, and so the catalyst layer of step (4) is deposited on the protective layer.

Accordingly, portions of the protective layer corresponding to the display pixels are further removed by dry etching between steps (9) and (10). In addition, in step (7), a layer of negative feedback resistance is deposited on the carbon nanotube arrays first, and then cathode electrodes are deposited on the layer of negative feedback resistance. The manufacturing material of the layer of negative feedback resistance is silicon or alloy.

The manufacturing material used in the protective layer of the gate electrodes and the insulating intermediate film is selected from the group consisting of: glass, metal coated with an insulation layer, silicon, silicon oxide, ceramic material and mica. The manufacturing material should be capable of withstanding a temperature of about 700°C for growing carbon nanotubes. The thickness of the protective layer of the gate electrodes is in the range of 1μm~100μm; and the thickness of the insulating intermediate film is in the range of 1μm~1000μm, preferably 10μm~200μm. The manufacturing material of the insulation layer is selected from the group consisting of: glass, metal coated with an insulation layer, silicon, silicon oxide, ceramic material and mica. The thickness of the insulation layer is in the range of 1μm~10mm, preferably 10μm~500μm. The thickness of the protective layer is in the range of 10nm~1000nm. The thickness of the catalyst layer is in the range of 1nm~10nm, preferably 5nm.

The insulating intermediate film of the field emission display according to the present invention can be used to control the distance between the gate electrodes and the carbon nanotube arrays. The distance can be controlled manually so as to obtain a low threshold voltage of the gate electrodes. The carbon nanotube arrays of the present invention are obtained by chemical vapor deposition, and the emitters for emitting electrons are the ends of the carbon nanotubes close to the catalyst layer. Thus, the carbon nanotubes for

emitting electrons can achieve extremely good uniformity in heights over a large area, thereby achieving uniformity in the field emission performance of each pixel. Furthermore, the emitting ends do not contain impurities such as catalyst particles or amorphous carbon, and do not contain randomly distributed carbon nanotubes. Thus, the field emission performance is more stable and more uniform, thereby increasing the lifetime of the field emission display.

The present invention will be further disclosed below in conjunction with the accompanying drawings and embodiments of the present invention.

【Description of the Drawings】

FIG. 1 is a front view of a substrate with a plurality of apertures used for making a field emission display in accordance with the present invention;

FIG. 2 is a schematic view of depositing gate electrodes on the substrate having a protective layer thereon;

FIG. 3 is a schematic view of depositing an insulating intermediate layer on the gate electrodes shown in FIG. 2;

FIG. 4 is a schematic view of depositing a protective layer on the insulating intermediate layer shown in FIG. 3;

FIG. 5 is a schematic view of forming a catalyst layer on the protective layer shown in FIG. 4;

FIG. 6 is a schematic view of forming an insulation layer with spaces on the catalyst layer shown in FIG. 5;

FIG. 7 is a schematic view of growing carbon nanotube arrays within the spaces on the insulation layer shown in FIG. 6;

FIG. 8 is a schematic view of depositing a layer of negative feedback resistance on top of the carbon nanotube arrays shown in FIG. 7;

FIG. 9 is a schematic view of depositing cathode electrodes on the layer of negative feedback resistance shown in FIG. 8;

FIG. 10 is a schematic view of packaging the cathode electrodes with a

bottom cover after removing the substrate shown in FIG. 9;

FIG. 11 is a schematic view of etching on the insulating intermediate layer shown in FIG. 10 and the protective layer of the gate electrodes;

FIG. 12 is a schematic view of etching on the protective layer of the carbon nanotubes;

FIG. 13 is a schematic structural view of the field emission display having been packaged with a display screen.

【Embodiments of the Invention】

First referring to FIG. 13, this is a schematic structure view of the field emission display according to the present invention. The display comprises: the cathode electrodes 17, the anode electrodes 20, the gate electrodes 19 between the cathode electrodes 17 and the anode electrodes 20, carbon nanotube arrays 15 used as the emitting units, an insulation layer 14 between the gate electrodes 19 and the cathode electrodes 17, and an insulating intermediate film 12 between the insulation layer 14 and the gate electrodes 19. The first ends of the carbon nanotube arrays 15 and the cathode electrodes 17 are connected electrically by a layer of negative feedback resistance 16. The opposite second ends of the carbon nanotube arrays 15 are roughly coplanar with the surface of the insulation layer 14, which is close to the gate electrode 19. The cathode electrodes 17 are packaged with a bottom cover 18.

The method for fabricating the field emission display according to the present invention is illustrated below in conjunction with FIGS. 1-12.

Referring to FIG. 1, a substrate 10 is first provided. There can be tiny grooves or apertures on the surface of the substrate 10 for facilitating removal of the substrate 10 from the product. The surface is coated with a

material which can easily be removed, for example wax, so as to achieve a variation of less than 1μm in a flatness of the surface. The substrate 10 should be able to withstand the high temperature used for growing carbon nanotubes, and be used repeatedly.

Then a protective layer (not shown) is deposited on the substrate 10. The protective layer is for protecting gate electrodes 19 from carbon deposition in a later growing process. Whether or not the protective layer is formed for the gate electrodes 19, depends on the material of the gate electrodes 19. Thus, the formation of the protective layer is not an essential step in the present invention. The material of the protective layer for the gate electrodes 19 is the same as that of an insulating intermediate layer 11. The protective layer for the gate electrodes 19 has a thickness in the range of 1μm~100μm.

Referring to FIG. 2, then the gate electrodes 19 are deposited on the substrate 10 having the protective layer thereon. The deposition can be performed by e-beam evaporation, thermal evaporation or sputtering. The deposition can be formed using a mold (not shown) or a photolithography process. The gate electrodes 19 can be made of any metal theoretically, but the metal should be capable of withstanding a temperature of about 700°C for growing carbon nanotubes. Furthermore, the metal has a coefficient of thermal expansion compatible with those of the protective layer for the gate electrodes 19, the insulating intermediate layer 11, the protective layer 12, the insulation layer 14, the bottom cover 18, and the substrate 10.

Referring to FIG. 3, then an insulating intermediate layer 11 is deposited on the gate electrodes 19 by coating or printing. Alternatively, a prepared thin plate can be used as the insulating intermediate layer 11. The insulating intermediate layer 11 is for controlling the distance between the cathodes electrodes 17 and the gate electrodes 19, and is also used as a

substrate for printing and growing in a later process. The thickness of the insulating intermediate layer 11 is in the range of 1μm~1000μm, preferably 10μm ~ 200μm; and the variation in flatness of the insulating intermediate layer 11 is less than 1μm. The material of the insulating intermediate layer 11 should be capable of being processed by photolithography and withstanding a temperature of about 700°C for growing carbon nanotubes. The material can be glass capable of enduring high temperatures, metal coated with an insulation layer, silicon, silicon oxide, ceramic material, mica, and so on.

Referring to FIG. 4, then a protective layer 12 is deposited on the insulating intermediate layer 11. Display pixels are made by photolithography during deposition. The protective layer 12 is for protecting carbon nanotubes from being damaged during wet etching, which may be used in a later process. Thus, the protective layer 12 is not an essential structure of the present invention. The protective layer 12 is made of silicon or other materials, which are capable of being processed by a wet etching process, and which are removable by a dry etching process without damaging the carbon nanotubes. The deposition can be performed by e-beam evaporation or sputtering. The protective layer 12 is as thin as possible while fulfilling the requirement for protecting, and has a thickness in the range of 10nm~1μm.

Referring to FIG. 5, a catalyst layer 13 is then deposited on the protective layer 12. The material of the catalyst layer 13 can be transient elements, such as iron, cobalt, nickel, or their compounds. The deposition thickness of the catalyst layer 13 is in the range of 1nm~10nm, and preferably 5nm. The deposition may be performed by e-beam evaporation, thermal evaporation or sputtering.

Referring to FIG. 6, the insulation layer 14 is then formed on the

catalyst layer 13. The insulation layer 14 is for insulating the gate electrodes 19 from the cathode electrodes 17, and for defining spaces 141 for growing carbon nanotubes. The insulation layer 14 can be formed by coating or printing. A prepared thin plate can be used as the insulation layer 14. The thickness of the insulation layer 14 depends on heights of the carbon nanotube arrays 15 and is in the range of 1μm~10mm, preferably 10μm~500μm. For the prepared thin plate, the surface of the plate facing the catalyst layer has a variation in flatness of less than 1μm. Display pixels should be made during this step. The material of the insulation layer 14 should be capable of withstanding a temperature of about 700°C for growing carbon nanotubes. The material can be glass capable of withstanding high temperatures, metal coated with an insulation layer, silicon, silicon oxide, ceramic material, mica, and so on.

Referring to FIG. 7, the carbon nanotube arrays 15 are then grown in the spaces 141 defined by the insulation layer 14. The heights of the carbon nanotube arrays 15 are approximately equal to the thickness of the insulation layer 14. The unevenness in heights of the carbon nanotube arrays does not influence the field emission display performance.

Referring to FIG. 8, the layer of negative feedback resistance 16 then can be formed optionally, depending on the needs of the driving circuit. The material of the layer has a proper resistivity, and can for example be silicon or an alloy. The thickness of the layer depends on the resistance needed. The resistance is determined by the designed circuit and the working voltage of the gate electrodes, and may range from 1KΩ to 100MΩ. The deposition can be performed by e-beam evaporation, thermal evaporation or sputtering. The shape of the deposition is the same as the cathode electrodes, and the deposition requires a mold.

Referring to FIG. 9, the cathode electrodes 17 are deposited on the layer

of negative feedback resistance 16. The deposition method is the same as that of the layer of negative feedback resistance 16, and the same deposition template is used in both depositions. The material of the cathode electrodes 17 is the same as that of the gate electrodes 19.

Referring to FIG. 10, the cathode electrodes 17 are packaged with a bottom cover 18. The bottom cover 18 can be made of glass, plastic, ceramic material, and so on. The bottom cover 18 is made by printing, bonding or fusion, etc.

Referring to FIG. 11, the substrate 10 is removed. Then, portions of the protective layer for the gate electrodes 19 and the insulating intermediate layer 11 are removedby a proper process; for example, a wet etching process. The removed portions correspond to the display pixels (not shown).

Referring to FIG. 12, then portions of the protective layer 12 corresponding to the display pixels (not shown) are removed by a proper process; for example, a dry etching process. A laser may be used to remove the catalyst layer 13 if necessary.

Referring to FIG. 13, the above-obtained structure is packaged together with a display screen, whereby a field emission display is completed. The display screen comprises the anode electrodes 20, a glass substrate 21, and a phosphor layer 22.

It is understood that the invention may be embodied in other forms without departing from the spirit thereof. Thus, the present examples and embodiments are to be considered in all respects as illustrative and not restrictive, and the invention is not to be limited to the details given herein.

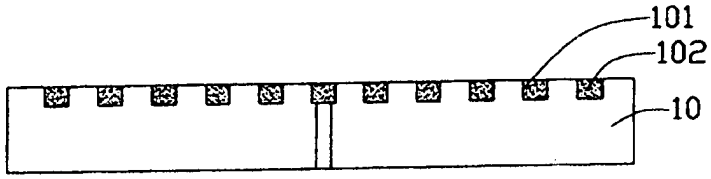

FIG. 1

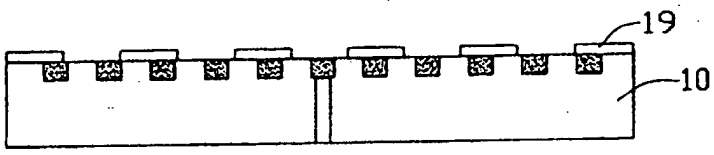

FIG. 2

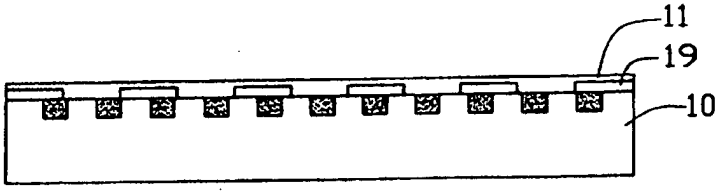

FIG. 3

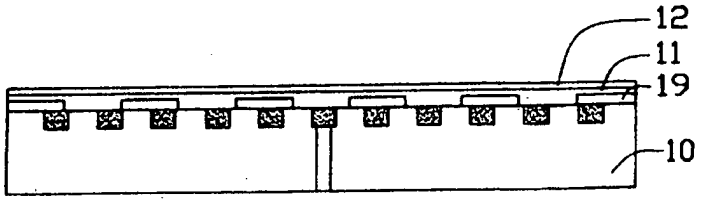

FIG. 4

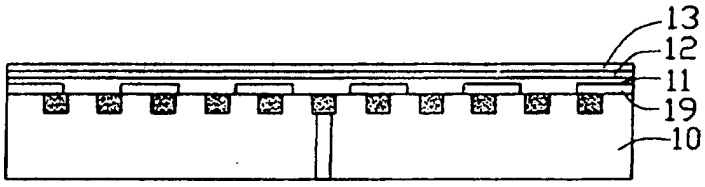

FIG. 5

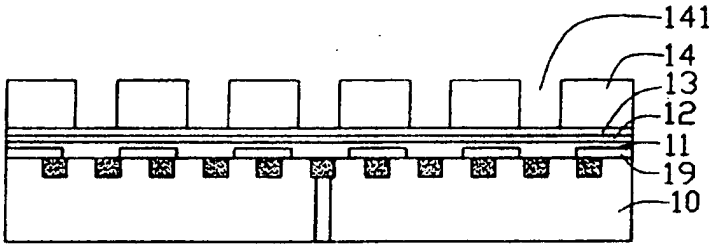

FIG. 6

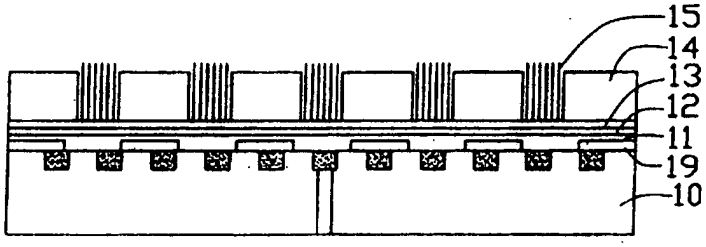

FIG. 7

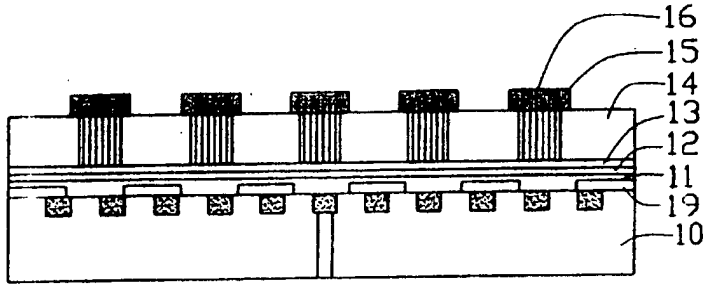

FIG. 8

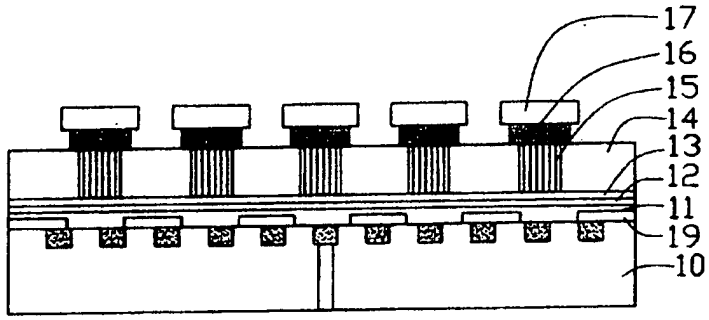

FIG. 9

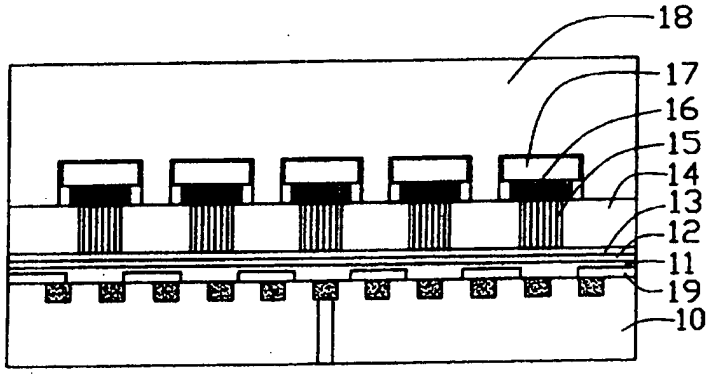

FIG. 10

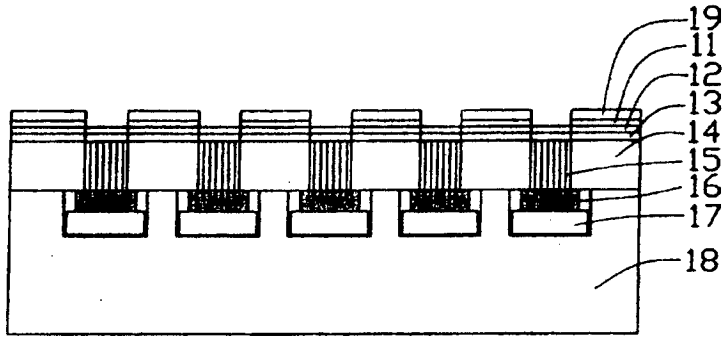

FIG. 11

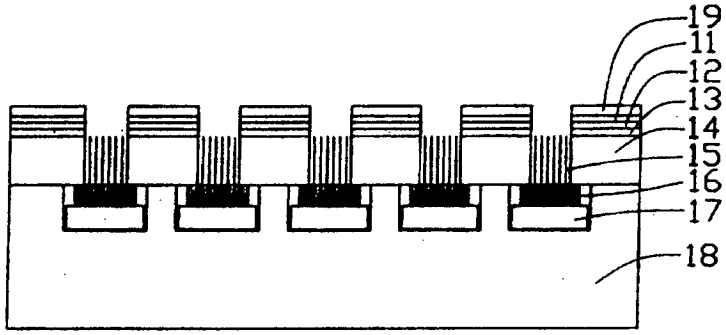

FIG. 12

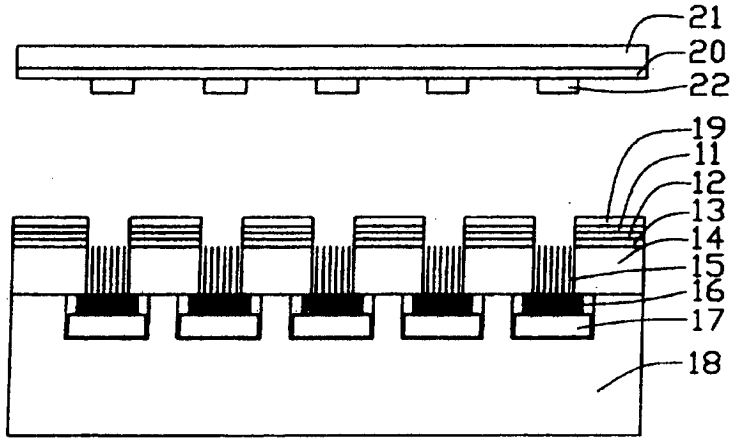

FIG. 13